

Development Tools (1/5)

Remark For details about development tools, see the site for development tools at NEC Electronics Website.
NEC Electronics Website: <http://www.necel.com>

(1) Software Tools

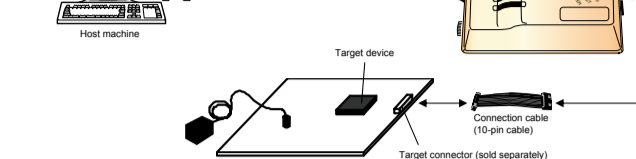
Host Machine	Software Tools
IBM PC/AT compatibles, PC98-NX-series	Software package: SP78K0 Assembler package: RA78K0 C compiler: CC78K0 C library source file: C78K0.L Integrated debugger: ID78K0-GB System emulator: SM+ for 78K0K2 Device file: DF78047

(2) Hardware Tools (1/3)

<1> On-chip debug emulator QB-78K0MINI (MINICUBE®)

On-chip Debug Emulator	Target Connector Specifications
QB-78K0MINI	10-pin general-purpose connector (2.54 mm pitch)

Remark The QB-78K0MINI is supplied with ID78K0-GB, a USB cable, a connection cable (10-pin cable) and a self-check board.



Connector pin layout (10-pin)

Pin No.	Pin Name	Pin Description
1	RESET_IN	Pin used to input reset signal from the target system
2	RESET_OUT	Pin used to output reset signal to the target device
3	FLMDD	Output pin used to control on-chip debugging functions
4	VDD	Input pin for when using power supply of the target system
5	X2DATA	Pin used to input/output for data communication during debugging
6	ND	Connected to GND.
7	X1CLK	Pin used to output clock signal to the target device
8	GND	Connected to GND.
9	RESERVED	Open
10	RESERVED	Open

Notes 1. Signal names in MINICUBE.
2. As seen from MINICUBE.

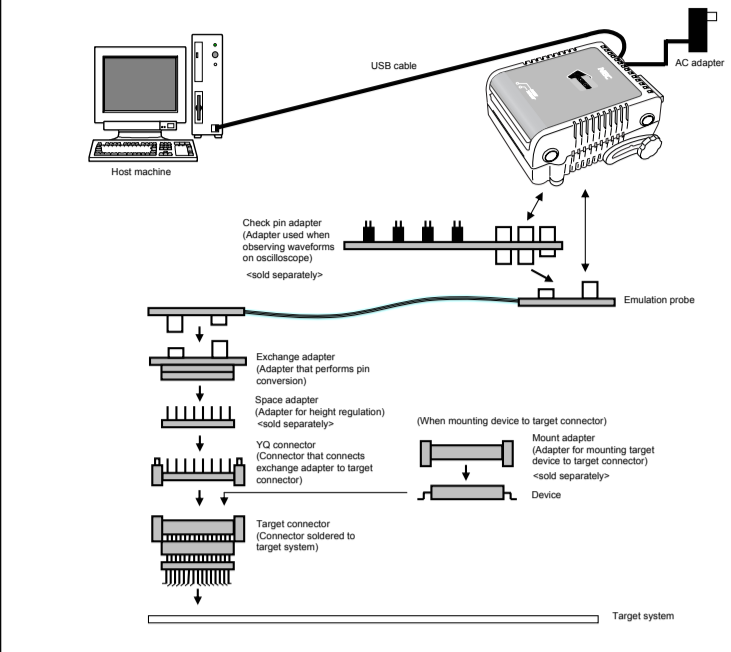
Development Tools (2/5)

(2) Hardware Tools (2/3)

<2> In-circuit emulator QB-78K0K2 (IECUBE®)

In-Circuit Emulator	Package	Check Pin	Emulation Probe	Exchange Adapter	Space Adapter	YQ Connector	Mount Adapter	Target connector
QB-78K0K2	80-pin PLCC (144 pins)	QB-144-CA-01	QB-85-EP-01T	QB-800C-EA-01T	QB-800C-YB-01T	QB-800C-YQ-01T	QB-800C-HA-01T	QB-800C-NO-01T
	80-pin PLCC (144 pins)			QB-800C-EA-01T	QB-800C-YB-01T	QB-800C-YQ-01T	QB-800C-HA-01T	QB-800C-NO-01T

Remark The QB-78K0K2 is supplied with ID78K0-GB, a USB cable, a power supply unit, QB-MIN2, connection cables (10-pin cable and 16-pin cable) and the 78K0-OCB board.



Notes 1. Signal names in MINICUBE.
2. As seen from MINICUBE.

Development Tools (3/5)

(2) Hardware Tools (3/3)

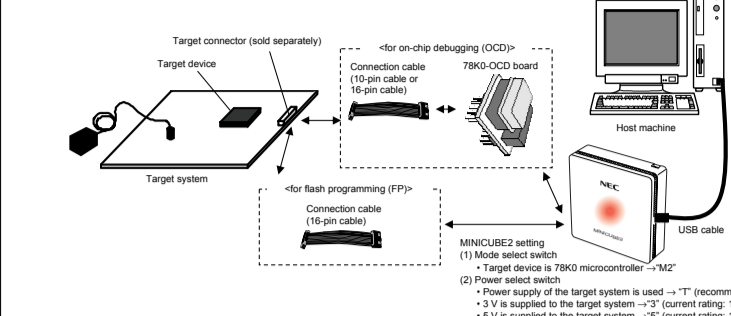
<2> On-chip debug emulator with programming function QB-MIN2 (MINICUBE®) for on-chip debugging

On-Chip Debug Emulator with Programming Function	Target Connector Specifications
QB-MIN2	10-pin general-purpose connector (2.54 mm pitch) When using 10-pin cable 16-pin general-purpose connector (2.54 mm pitch) When using 16-pin cable

(3) Flash Memory Write Tools (1/3)

<1> On-chip debug emulator with programming function QB-MIN2 (MINICUBE®) for flash programming

Remarks 1. The QB-MIN2 is supplied with a USB cable, connection cables (10-pin cable and 16-pin cable) and the 78K0-OCB board.
2. A connection cable (10-pin cable) and the 78K0-OCB board are used only when using the on-chip debug function.
3. The software is required separately to operate QB-MIN2.
4. Download the latest software from our website (<http://www.necel.com>), and use it.



Connector pin layout (16-pin)

Pin No.	Pin Name	Pin Description
1	GND	Connected to GND.
2	RESET_IN	Pin used to input reset signal to the target device
3	RESERVED (during OCB)	Open
4	RESERVED (during OCB)	Open
5	VDD	Input pin for when using power supply of the target system
6	RESERVED (during OCB)	Open
7	RESERVED (during OCB)	Open
8	CLK	Pin used to output clock signal to the target device
9	RESERVED	Open
10	RESERVED	Open
11	DATA (during OCB)	Pin used to input/output for data communication during debugging
12	RESERVED (during OCB)	Open
13	DATA (during OCB)	Pin used to input/output for data communication during debugging
14	FLMDD	Output pin used to control on-chip debugging functions
15	RESET_IN (during OCB)	Pin used to input reset signal from the target system
16	RESERVED	Open

Notes 1. Signal names in MINICUBE.
2. As seen from MINICUBE.
3. The 10-pin target connector is the same as that of MINICUBE. See the description of the target connector of MINICUBE.

Development Tools (4/5)

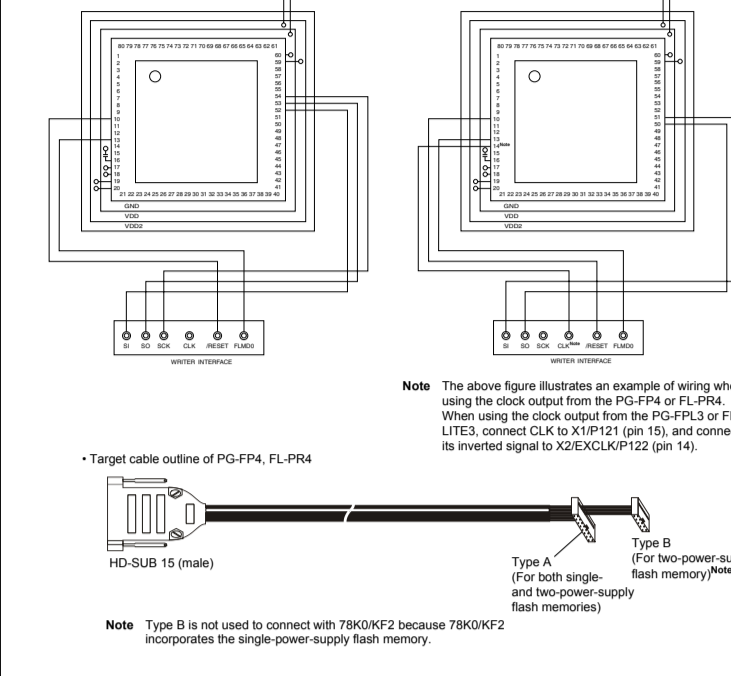
(3) Flash Memory Write Tools (2/3)

<2> Flash memory programmer PG-FP4, FL-PR4, PG-FLP3, FL-LITE3 (1/2)

Flash Memory Programmer	Flash Memory Adapter	Flash Memory Write Adapter
Flash memory programmer: PG-FP4, FL-PR4 Simple flash memory programmer: PG-FLP3, FL-LITE3	FA-800K-BT-A FA-78F047OC-LIB-MK FA-800K-EU-A	80-pin plastic LQFP (14x14) 80-pin plastic LQFP (pin pitch) (12x12)

Remarks 1. FL-PR4, FL-LITE3, FA-800K-BT-A, FA-78F047OC-LIB-MK, FA-800K-EU-A, and FA-78F047OC-BEUM-A are products of Naito Denso Machida Mfg. Co., Ltd.
TEL: +81-42-750-4122 Naito Denso Machida Mfg. Co., Ltd.
2. Use the latest version of the flash memory programming adapter.

• Wiring example in 3-wire serial IO (CS10) mode
• Wiring example in UART (UART6) Mode



Note The above figure illustrates an example of wiring when using the clock output from the PG-FP4 or FL-PR4. When using the clock output from the PG-FLP3 or FL-LITE3, connect CLK to X1P121 (pin 15), and connect its inverted signal to X2/EXCLKP122 (pin 14).

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(3) Flash Memory Write Tools (3/3)

<2> Flash memory programmer PG-FP4, FL-PR4, PG-FLP3, FL-LITE3 (2/2)

Connector pin layout of PG-FP4 and FL-PR4 (view from socket side)

Pin No.	Pin Name	Pin Description					
1	3	5	7	9	11	13	15
2	4	6	8	10	12	14	16

Connector pin configuration of PG-FP4 and FL-PR4

Signal Name of PG-FP4	Target Connector Type A Signal (16-Pin)
GND	1
RESET	2
FLMDD	3
VDD	4
SOT1D	5
SOCK	7
CLK	8
RESERVED	9
RESERVED	10
RESERVED	11
RESERVED	12
RESERVED	13
RESERVED	14
RESERVED	15
RESERVED	16

Note Signals in parentheses and the corresponding pins are not used with 78K0KF2.

Operation List (1/6)

Operand Identifiers and specification methods

Identifier	Specification Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), L (R5), H (R7), AX (R6), BC (R8), DE (R9), F (R10), H (R11)
sp	Special function register symbol ^{*)}
addr	Special function register symbol bit manipulating behavior even addresses only ^{*)}
addr	F2E0 to F1F1 Immediate data or labels
addr	F2E0 to F1F1 Immediate data or labels (even address only)
addr16	0000 to FFFF Immediate data or labels (Only even addresses for 16-bit data transfer instructions)
addr16	0000 to FFFF Immediate data or labels
addr16	0000 to FFFF Immediate data or labels (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
Rbn	R0 to R8

Note Addresses from FFD0H to FFD0H cannot be accessed with these operands.

Operation List (2/6)

Description of operation column
A: A register, B: B register, C: C register, D: D register, E: E register, H: H register, L: L register, AX: AX register pair, BC: BC register pair, DE: DE register pair, HL: HL register pair, PC: Program counter, SP: Stack pointer, PSW: Program status word, CY: Carry flag, AC: Auxiliary carry flag, Z: Zero flag, RS: Register bank select flag, IE: Interrupt request enable flag, () Memory contents indicated by address or register contents in parentheses, Ac: Ac, Higher 8 bits and lower 8 bits of 16-bit register, ~: Logical product (AND), ~: Logical sum (OR), ~: Exclusive logical sum (exclusive OR), ~: Inverted data, addr16: 16-bit immediate data or label, #addr: Signed 8-bit displacement value

Instruction Group	Mnemonic	Operands	Bytes	Notes 1	Notes 2	Operation	Flag
16-bit data transfer	MOV	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
16-bit data transfer	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access
2. When an area except the internal high-speed RAM area is accessed
3. Except "r = A"

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{clk}) selected by the processor clock control register (PCC).
2. This clock cycle applies to the internal ROM program.

Operation List (3/6)

Description of operation column
A: A register, B: B register, C: C register, D: D register, E: E register, H: H register, L: L register, AX: AX register pair, BC: BC register pair, DE: DE register pair, HL: HL register pair, PC: Program counter, SP: Stack pointer, PSW: Program status word, CY: Carry flag, AC: Auxiliary carry flag, Z: Zero flag, RS: Register bank select flag, IE: Interrupt request enable flag, () Memory contents indicated by address or register contents in parentheses, Ac: Ac, Higher 8 bits and lower 8 bits of 16-bit register, ~: Logical product (AND), ~: Logical sum (OR), ~: Exclusive logical sum (exclusive OR), ~: Inverted data, addr16: 16-bit immediate data or label, #addr: Signed 8-bit displacement value

Instruction Group	Mnemonic	Operands	Bytes	Notes 1	Notes 2	Operation	Flag
16-bit data transfer	MOV	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
16-bit data transfer	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY
	MOVB	r, #byte addr, #byte	2 3	2	8	r ← byte (addr) ← byte	Z AC CY
	MOVW	r, #word addr, #word	4 5	2	16	r ← word (addr) ← word	Z AC CY

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access
2. When an area except the internal high-speed RAM area is accessed
3. Except "r = A"

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{clk}) selected by the processor clock control register (PCC).
2. This clock cycle applies to the internal ROM program.

Operation List (4/6)

Description of operation column
A: A register, B: B register, C: C register, D: D register, E: E register, H: H register, L: L register, AX: AX register pair, BC: BC register pair, DE: DE register pair, HL: HL register pair, PC: Program counter, SP: Stack pointer, PSW: Program status word, CY: Carry flag, AC: Auxiliary carry flag, Z: Zero flag, RS: Register bank select flag, IE: Interrupt request enable flag, () Memory contents indicated by address or register contents in parentheses, Ac: Ac, Higher 8 bits and lower 8 bits of 16-bit register, ~: Logical product (AND), ~: Logical sum (OR), ~: Exclusive logical sum (exclusive OR), ~: Inverted data, addr16: 16-bit immediate data or label, #addr: Signed 8-bit displacement value

Instruction Group	Mnemonic	Operands	Bytes	Notes 1	Notes 2	Operation	Flag
8-bit operation	OR	r, #byte addr, #byte	2 3	2	8	r ← r OR byte (addr) ← (addr) OR byte	Z AC CY
	AND	r, #byte addr, #byte	2 3	2	8	r ← r AND byte (addr) ← (addr) AND byte	Z AC CY
	XOR	r, #byte addr, #byte	2 3	2	8	r ← r XOR byte (addr) ← (addr) XOR byte	Z AC CY
	AND	r, #byte addr, #byte	2 3	2	8	r ← r AND byte (addr) ← (addr) AND byte	Z AC CY
	OR	r, #byte addr, #byte	2 3	2	8	r ← r OR byte (addr) ← (addr) OR byte	Z AC CY
	XOR	r, #byte addr, #byte	2 3	2	8	r ← r XOR byte (addr) ← (addr) XOR byte	Z AC CY
	AND	r, #byte addr, #byte	2 3	2	8	r ← r AND byte (addr) ← (addr) AND byte	Z AC CY
	OR	r, #byte addr, #byte	2 3	2	8	r ← r OR byte (addr) ← (addr) OR byte	Z AC CY
	XOR	r, #byte addr, #byte	2 3	2	8	r ← r XOR byte (addr) ← (addr) XOR byte	Z AC CY
	AND	r, #byte addr, #byte	2 3	2	8	r ← r AND byte (addr) ← (addr) AND byte	Z AC CY
16-bit operation	OR	r, #word addr, #word	4 5	2	16	r ← r OR word (addr) ← (addr) OR word	Z AC CY
	AND	r, #word addr, #word	4 5	2	16	r ← r AND word (addr) ← (addr) AND word	Z AC CY
	XOR	r, #word addr, #word	4 5	2	16	r ← r XOR word (addr) ← (addr) XOR word	Z AC CY
	AND	r, #word addr, #word	4 5	2	16	r ← r AND word (addr) ← (addr) AND word	Z AC CY
	OR	r, #word addr, #word	4 5	2	16	r ← r OR word (addr) ← (addr) OR word	Z AC CY
	XOR	r, #word addr, #word	4 5	2	16	r ← r XOR word (addr) ← (addr) XOR word	Z AC CY
	AND	r, #word addr, #word	4 5	2	16	r ← r AND word (addr) ← (addr) AND word	Z AC CY
	OR	r, #word addr, #word	4 5	2	16	r ← r OR word (addr) ← (addr) OR word	Z AC CY
	XOR	r, #word addr, #word	4 5	2	16	r ← r XOR word (addr) ← (addr) XOR word	Z AC CY
	AND	r, #word addr, #word	4 5	2	16	r ← r AND word (addr) ← (addr) AND word	Z AC CY

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access
2. When an area except the internal high-speed RAM area is accessed
3. Except "r = A"

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{clk}) selected by the processor clock control register (PCC).
2. This clock cycle applies to the internal ROM program.

Operation List (5/6)

Description of operation column
A: A register, B: B register, C: C register, D: D register, E: E register, H: H register, L: L register, AX: AX register pair, BC: BC register pair, DE: DE register pair, HL: HL register pair, PC: Program counter, SP: Stack pointer, PSW: Program status word, CY: Carry flag, AC: Auxiliary carry flag, Z: Zero flag, RS: Register bank select flag, IE: Interrupt request enable flag, () Memory contents indicated by address or register contents in parentheses, Ac: Ac, Higher 8 bits and lower