

# A Study of Folding and Interpolating ADC

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**Abstract**—An architectural exploration and analysis of performance limitations in folding/interpolation analog-to-digital converters (ADCs) is presented. The analysis is based on a behavioral MATLAB/SIMULINK model, which captures non-idealities such as mismatch and non-linearity in the folding amplifiers, interpolation network and comparators. The focus of the study has been placed on the design trade-offs in direct and cascaded folding architectures in CMOS operating at low supply voltages. We propose the differential folding and an efficient radix-5, 2-stage cascaded architecture. In addition, we propose a novel bit alignment scheme that can be used for the cascaded folding structure, which greatly reduces the total number of comparators, which is only  $5+5+12=22$  for an 8-bit prototype. Monte-Carlo simulation is performed and results are summarized.

## I. INTRODUCTION

With the rapid expansion of broadband digital communication over the past two decades, medium and low-resolution analog-to-digital converters (ADCs) attract a lot of attentions as one of the most important building blocks for the analog front-end. Flash and folding/interpolating architectures stand as the main choices due to their amenability to the continuous device scaling of the digital CMOS process.

Compared to the flash architecture, where the hardware complexity is proportional to  $2^n$  ( $n$  is the resolution bits), the use of folding reduces the number of comparators by  $2^m$  ( $m$  is the folding factor). Comparator number reduction stems from the fact that each comparator is used more than once. In addition to folding, interpolation further reduces the number of preamps required for the fine quantizer. This converter inherits the one-step nature of the flash converter yet greatly reduces the hardware complexity. Therefore it is generally believed to be a smart replacement of the flash architecture.

This report is organized as follows. In section 2 we present direct and cascaded ADC architectures. Design tradeoffs in cascaded architecture are presented and discussed in section 3. Summary of the simulation results and comparative performance analysis is given in section 4. Section 5 concludes the report.

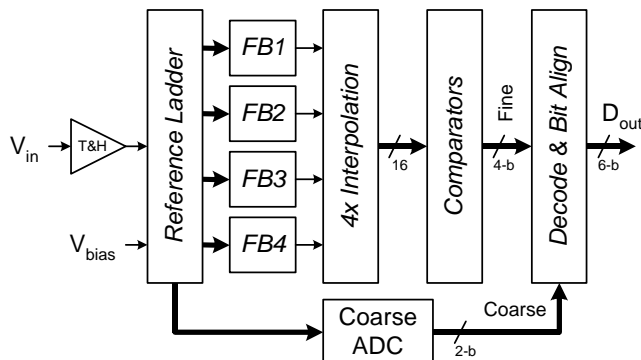


Fig. 1. A 6-bit folding/interpolating ADC.

## II. ARCHITECTURAL EXPLORATION

Two ADC architectures are analyzed. The first one uses a 6-bit conventional one-stage (direct) folding structure. The second architecture employs cascaded folding. An 8-bit prototype is designed and modeled.

### A. Direct Architecture

The system is partitioned into a 2-b coarse and a 4-b fine sub-converters as shown in Fig. 1. Main building blocks are summarized below.

**Fine (4-bit) ADC:** The folder contains 4 banks of folding amplifiers. Each of them has a folding factor of 4 and contains 5 differential pairs. Mathematical model of the non-linearity of the folding amplifier is constructed based on the square-law saturation characteristic of a MOSFET differential pair. The nonlinear transfer function is cascaded by a finite bandwidth RC load.

**Coarse (2-bit) ADC:** A parallel 2-b coarse ADC is constructed. It contains two MSB comparators placed close to  $1/4$  and  $3/4$  of the full scale. The coarse comparator can tolerate very large offset in that its decision is only used as an indicator to resolve the ambiguity inherent in the folding signal.

**Bit alignment:** Due to the built-in parallelism in the fine and coarse sub-converters, their decisions at the proximity of the MSB's may not agree due to random offsets and timing error. Bit alignment logic is designed to solve this problem.

### B. Cascaded Architecture

First we note that a large folding factor developed in a single-stage folding architecture reduces the number of comparators at the cost of an increased capacitive loading at the folder output, and therefore limits the analog bandwidth. Large folding factor is also difficult to realize in one-step architecture because it is hard to avoid overlapping of linear operation ranges between adjacent folding differential pairs. This problem is more prominent in CMOS technology as opposed to bipolar in that the  $V_{DSAT}$  value of a MOSFET is usually much larger than the  $V_i$  ( $=kT/q$ ) of a BJT. Furthermore, the supply voltage scaling of CMOS circuits exacerbates this problem as the input signal swing is reduced.

In contrast, if cascaded folding is employed, all the folds do not need to be generated in one step, allowing a more convenient value of  $V_{DSAT}$  to be used. At the same time, the excess capacitive loading due to inactive folding amplifiers is low. Furthermore, cascading gain stages helps to reduce the input-referred offset and non-linearity contribution from the back-end stages, especially the comparators. The metastable region of the comparators is also reduced by the distributed gain.

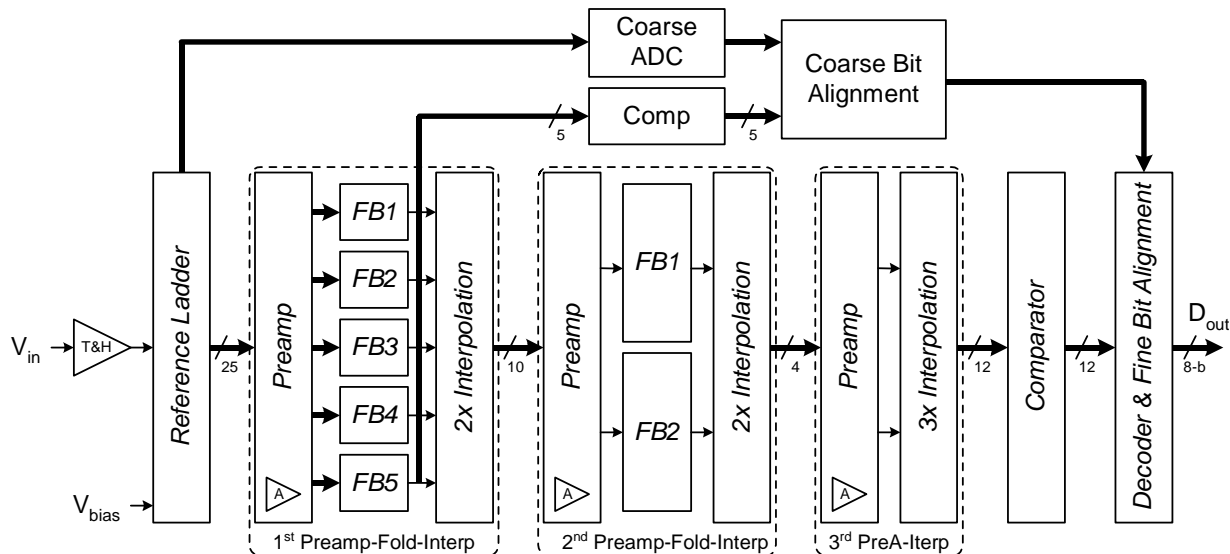


Fig. 2. An 8-bit cascaded folding/interpolating ADC.

To demonstrate feasibility of the proposed architecture, an 8-b prototype is designed (Fig. 2). Descriptions of the design tradeoffs associated with this architecture are given in the following section.

### III. DESIGN TRADEOFFS

#### A. Differential Folding

Conventional folding architecture dictates single-ended input and reference voltages. This reduces the noise tolerance at the input where the signal is most susceptible to substrate noise and unwanted signal coupling. A fully differential, double balanced folding structure is constructed, as depicted in Fig. 3.

#### B. Cascaded Folding Factor

As pointed out before, a low folding factor in one folding stage is preferred for implementation under low supply voltages; but a too low folding factor results in reduced saving in the number of comparators. In [7], a folding factor of 3 is used, which results in a large number of parallel folders and a large number of comparators required. It compromises the advantage of the folding idea and greatly increases the input capacitive loading (4.5pF).

Two known architectures facilitate the implementation of cascaded folding. One is called “parallel cascaded folding”

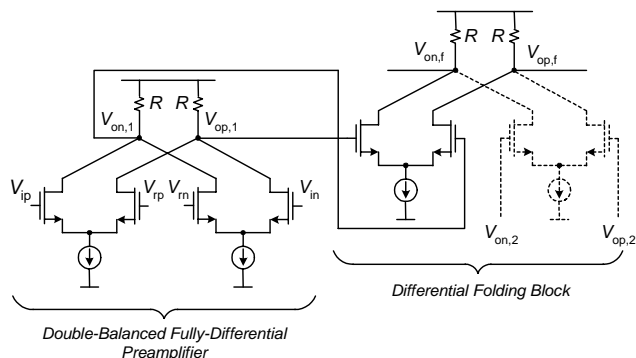


Fig. 3. Fully differential folding amplifier (preamp + folder)

[8], and the other one utilizes analog multipliers [8]. At low supply voltages, analog multipliers are difficult to design due to stacking cascode devices. In our approach, a parallel cascaded folding structure with a folding factor of 5 is chosen as a good compromise as our design is targeted to a low supply voltage of 1.5-V in a 0.18- $\mu$ m digital CMOS process. Two-stage folding results in a total folding factor of 25, which results in a fine ADC consisting of only 12 comparators.

#### C. Interpolation Non-linearity

Since folding ADC only requires accurate zero-crossings, little attention is usually paid to linearize the voltage transfer function of the folding amplifier. As a result, interpolation at the vicinity of the non-linear region distorts the zero-crossing point of the descendent signals. However, a differential architecture possessing odd symmetry introduces no error when an interpolation factor of 2 is used. This situation is worse in a cascaded structure in that interpolation non-linearity is further inherited by the succeeding stages. In our approach, an interpolation factor of 2 is chosen for the resistive interpolation of the first two stages. The third stage implements an interpolation factor of 3 since the required accuracy is low at this point. Improved resistive interpolation schemes may further improve the linearity of the ADC [8].

#### D. Distributed Gain

An inherent advantage of the cascaded structure is that a large gain can be developed in a gradual fashion. Each stage possesses a large bandwidth and contributes a moderate gain, resulting in a large overall gain and a large overall bandwidth. This approach takes advantage of the open-loop architecture and optimizes the bandwidth of analog preprocessing, yielding an improved dynamic performance of the converter.

#### E. Cascaded Bit Alignment

Bit alignment in direct folding structure is straightforward by placing “pointers” in between transition points of fine folding signals. Direct mapping of this idea to cascaded

folding case results in a brute-force implementation where a large number of coarse comparators are needed. In our 8-bit case, this number would be  $5 \times 5 = 25$ . Furthermore, these comparators cannot tolerate an offset of more than  $1/25$  of the full input range. Otherwise, bit alignment error will occur. This translates into a large complexity in terms of both chip area and power consumption.

A closer look at the fine folding signal reveals the possibility of a two-step offset coarse-fine bit alignment scheme. In this approach, a total of  $5+5=10$  coarse comparators are used, resulting in a saving of 15 comparators. Only 5 of these comparators are required to have a small offset of 6 LSBs. The other 5 can tolerate an offset as large as  $1/5$  of the input range.

#### F. Input Sample & Hold Circuit

The intrinsic analog parallelism in folding/interpolating ADC requires good matching in propagation delay between parallel signal paths and a low clock skew. This requirement can be very stringent in an 8-bit converter. A sample and hold circuit (S/H) operating at the front-end may greatly alleviate this problem. But for low supply voltages, the S/H stage may be saved at the cost of degraded performance for high-frequency input signals.

### IV. RESULTS

#### A. 6-bit, ADC

A 6-bit direct folding low complexity ADC is modeled. Please refer to our midterm report for details.

#### B. 8-bit ADC

Cascaded folding scheme is applied to an 8-bit ADC. The following two tables summarize the design constraints and performance of an 8-bit ADC for various circuit parameters according to SIMULINK simulation. The performance is obtained under the typical parameter values specified in Table 2. Fig. 8-12 illustrate performance of this ADC.

TABLE I: PERFORMANCE SUMMARY

Resolution	8.17-bit
# of decision levels	288
Missing code	No
Non-monotonic code	No
Full-scale input $V_{FS}$	$1V_{pp}$
DNL	$\pm 0.4\text{LSB}$
INL	$\pm 1\text{LSB}$
SFDR	58dB
SNDR	47.3dB

TABLE II: SUMMARY OF DESIGN CONSTRAINTS

Parameter	Constraint ( $3\sigma$ )
Ref. ladder matching	9-bit
1 <sup>st</sup> stage preamp gain matching	5-bit
2 <sup>nd</sup> stage preamp gain matching	4-bit
3 <sup>rd</sup> stage preamp gain matching	4-bit
1 <sup>st</sup> stage folder gain matching	5-bit
2 <sup>nd</sup> stage folder gain matching	4-bit
1 <sup>st</sup> stage intp. R matching	4-bit
2 <sup>nd</sup> stage intp. R matching	4-bit
3 <sup>rd</sup> stage intp. R matching	4-bit
Coarse comparator offset	100 mV
Middle comparator offset	50 mV
Fine comparator offset	20 mV

### V. CONCLUSION

A detailed study of folding and interpolation ADC architecture is performed. A case of an 8-bit cascaded folding ADC is modeled. Various circuit and architecture parameter tradeoffs are evaluated. It is found that the dominant non-linearity error in such a converter is still the mismatch of the reference resistor ladder and the offset of the input preamps. Interpolation greatly improves DNL; however, offers little help on INL. Cascaded folding is an efficient architecture for low complexity low supply voltage implementations.

### VI. REFERENCES

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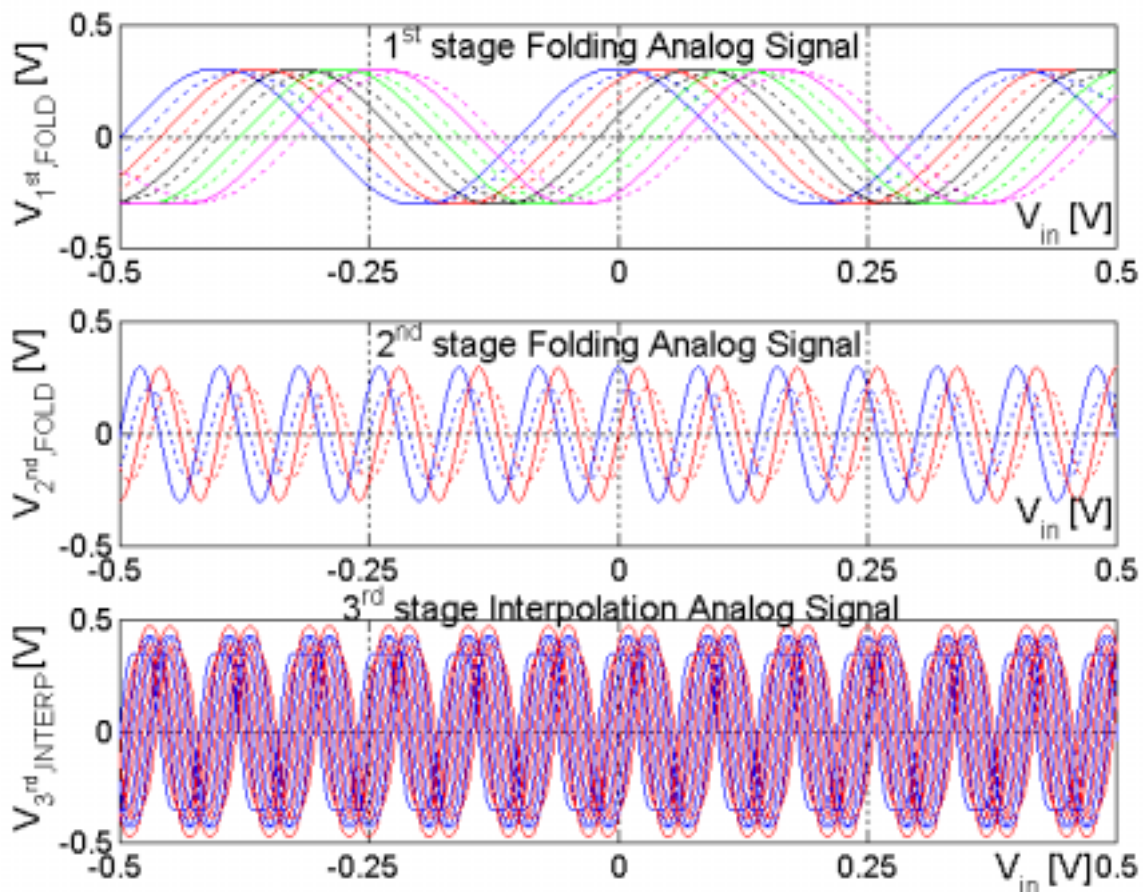


Fig. 8. Folding and interpolation signals in an 8-bit ADC.

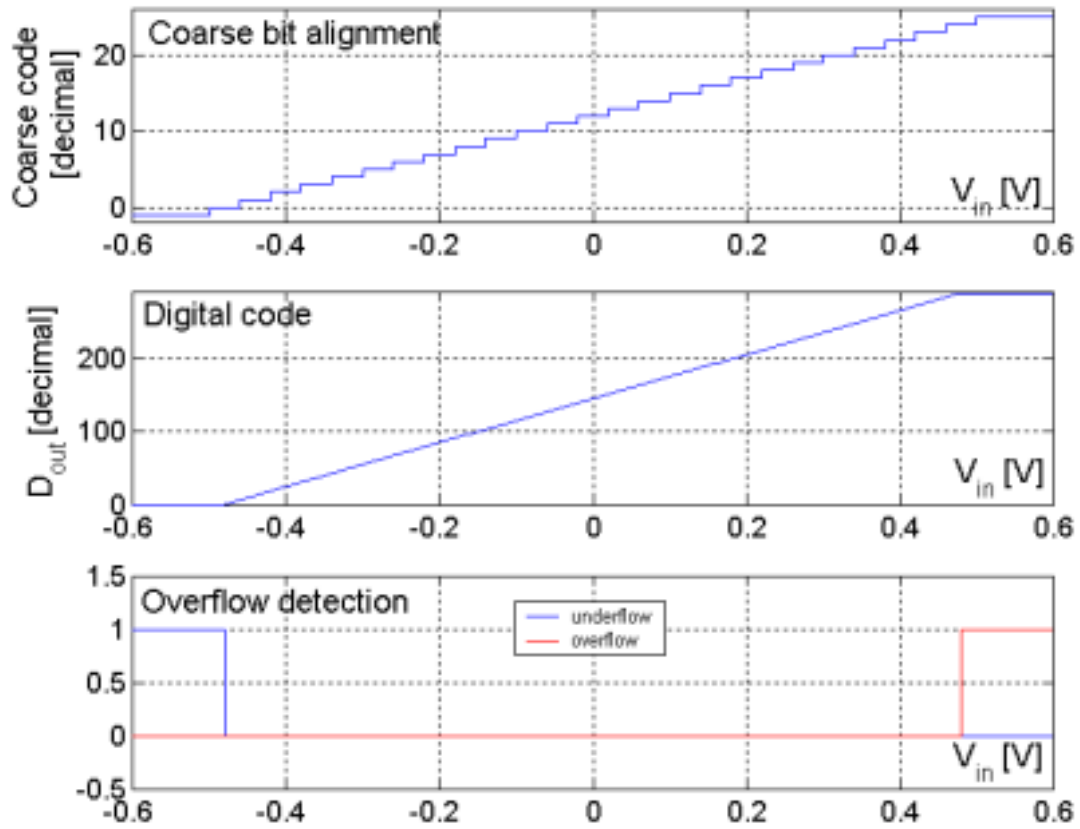


Fig. 9. 8-b ADC output due to ramp input.

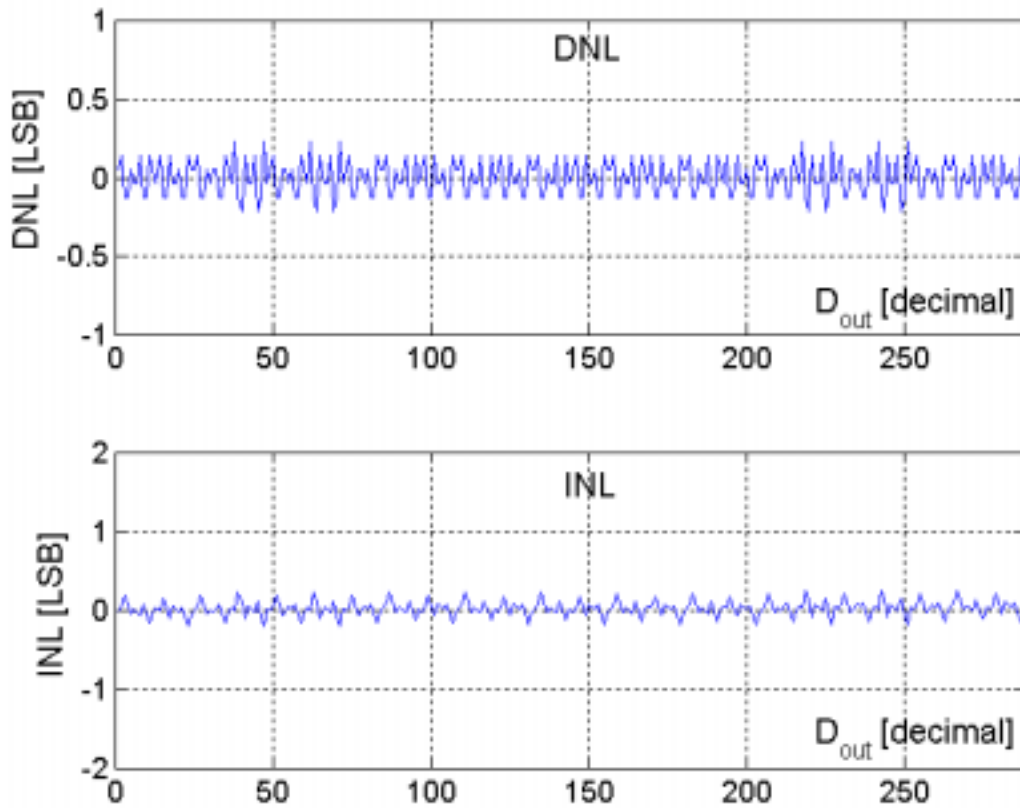


Fig. 10. 8-b AND DNL and INL under ideal parameter values.

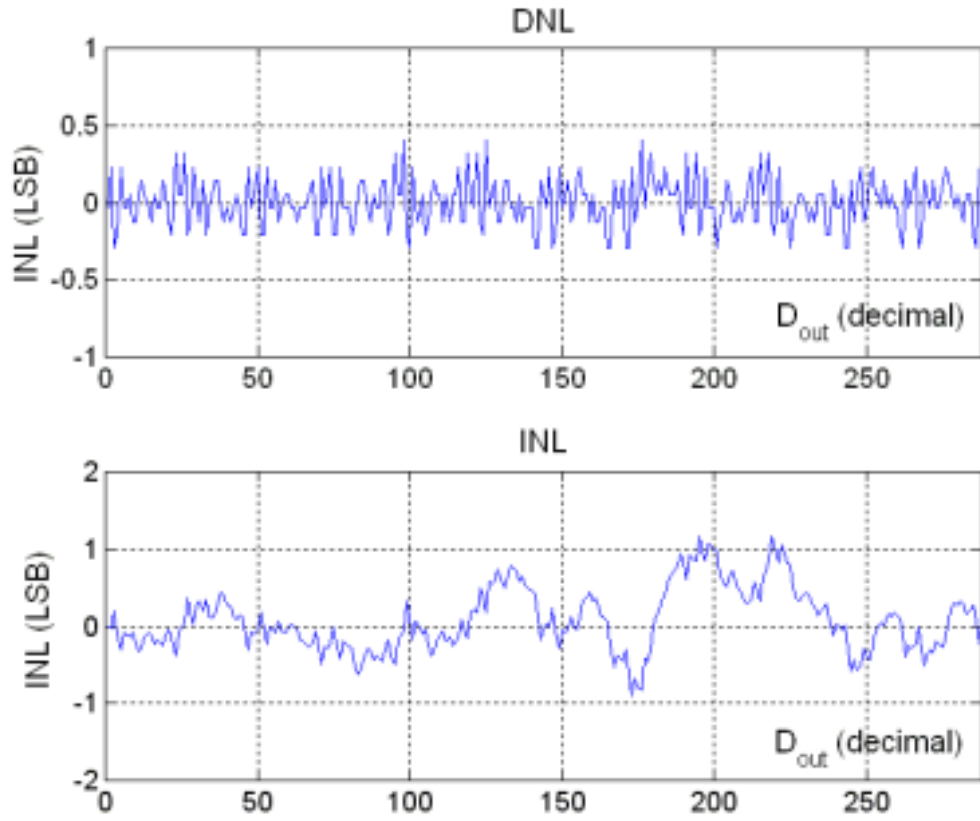


Fig. 11. 8-b ADC DNL and INL plot with circuit parameters specified in Table. 1.

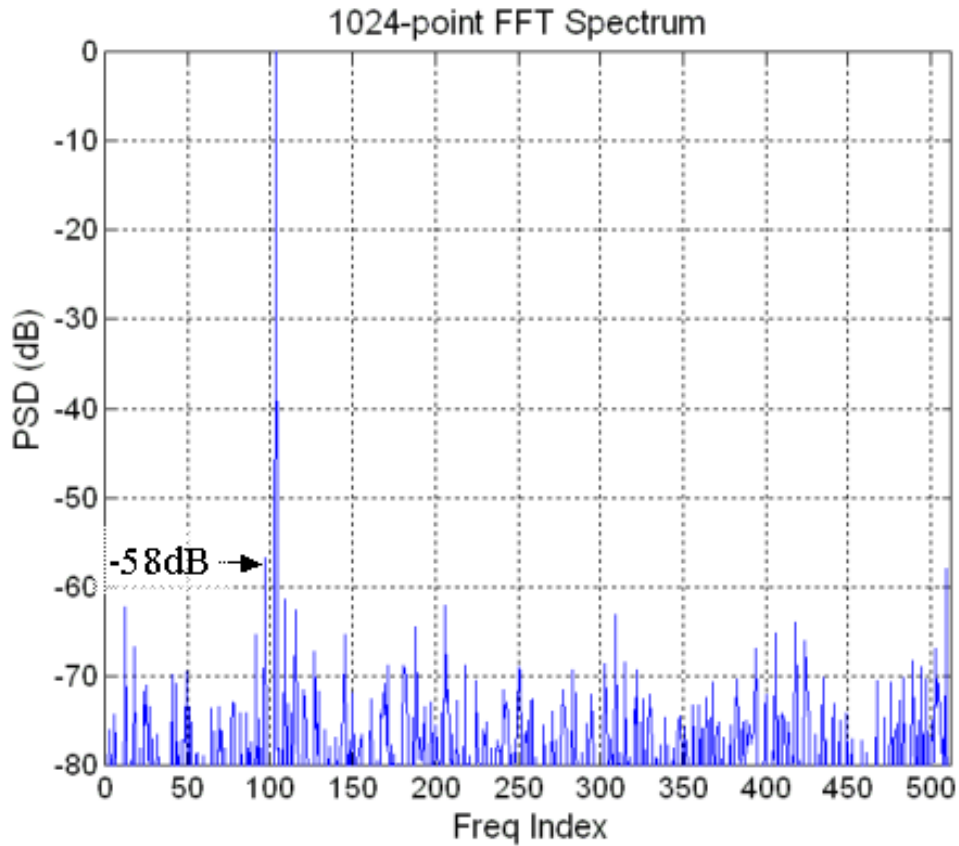


Fig. 12. Spectrum of the digitized sinusoidal input at 1/5 of the Nyquist frequency.

## FURTHER READING

Click any one of the following links to be taken to a website which contains the following documents.

The following are some recent examples of Asynchronous ADC activity off the web.

[6 bit Asynchronous December 2006](#)  
[Asynchronous ADC In CAD Mentor Graphics](#)  
[Asynchronous Data Processing System](#)  
[ASYNCHRONOUS PARALLEL RESISTORLESS ADC](#)  
[Flash Asynchronous Analog-to-Digital Converter](#)  
[Novel Asynchronous ADC Architecture](#)  
[LEVEL BASED SAMPLING FOR ENERGY CONSERVATION IN LARGE NETWORKS](#)  
[A Level-Crossing Flash Asynchronous Analog-to-Digital Converter](#)  
[Weight functions for signal reconstruction based on level crossings](#)  
[Adaptive Rate Filtering Technique Based on the Level Crossing Sampling](#)  
[Adaptive Level-Crossing Sampling Based DSP Systems](#)  
[A 0.8 V Asynchronous ADC for Energy Constrained Sensing Applications](#)  
[Spline-based signal reconstruction algorithm from multiple level crossing samples](#)  
[A New Class of Asynchronous Analog-to-Digital Converters](#)  
[Effects of time quantization and noise in level crossing sampling stabilization](#)

Here is some more background information on Analog to Digital converters.

[A 1-GS/s 6-bit 6.7-mW ADC](#)  
[A Study of Folding and Interpolating ADC](#)  
[Folding ADCs Tutorials](#)  
[high speed ADC design](#)  
[Investigation of a Parallel Resistorless ADC](#)

Here are some patents on the subject.

[4,291,299 Analog to digital converter using timed](#)  
[4,352,999 Zero crossing comparators with threshold](#)  
[4,544,914 Asynchronously controllable successive approximation](#)  
[4,558,348 Digital video signal processing system using](#)  
[5,001,364 Threshold crossing detector](#)  
[5,315,284 Asynchronous digital threshold detector](#)  
[5,945,934 Tracking analog to digital converter](#)  
[6,020,840 Method and apparatus for representing waveform](#)  
[6,492,929 Analogue to digital converter and method](#)  
[6,501,412 Analog to digital converter including a quantizers](#)  
[6,667,707 Analog to digital converter with asynchronous ability](#)  
[6,720,901 Interpolation circuit having a conversio2](#)  
[6,850,180 SelfTimed ADC](#)  
[6,965,338 Cascade A D converter](#)  
[7,133,791 Two mean level crossing time interval](#)

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